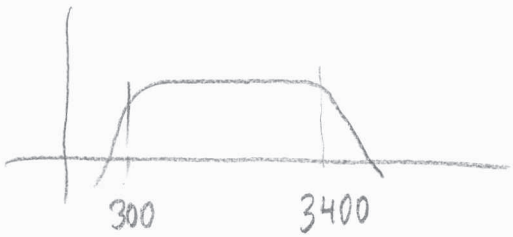
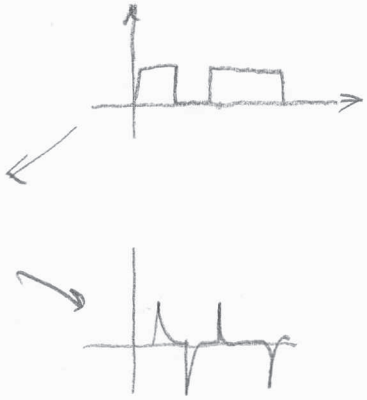
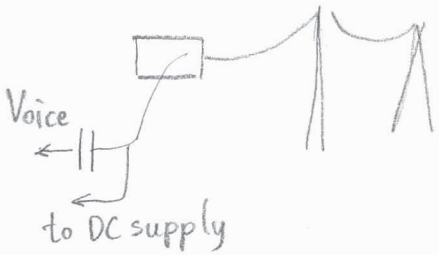
Phone line

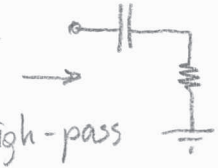


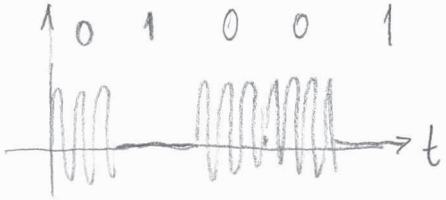




∴ Modulation Required !

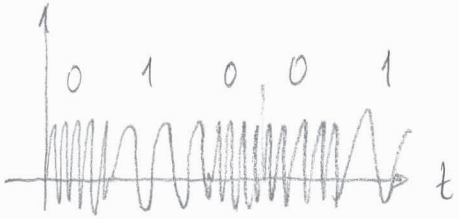
Equivalent cct



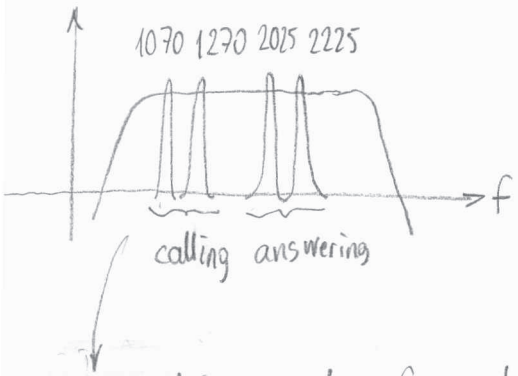


Amplitude Shift Keying

(is the bit 1 or the line is off?)



Phase Shift Keying



2 distinct frequencies → 1 symbol = 1 bit

4 frequencies → 1 symbol = 2 bits

general formula 1 symbol = $\log_2$ # of distinct signals
bits

Approximately 3 cyles for each frequency

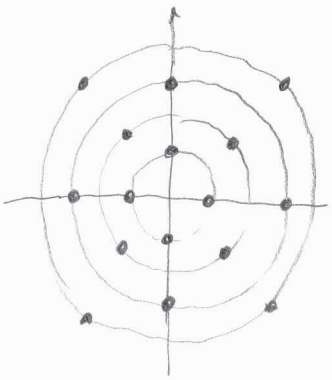
* the remote end detector can sense the received signal
* the BW is limited

→ Bit duration ~ 3 periods → bits/second $\tilde{=}$ 300 (considering the lowest freq.)

Modulation schemes

* Amplitude
* Frequency
* Phase

Circular 16-QAM



constellation diagram

# of bits per symbol = 4 ($\log_2 16$)

BAUD $\overset{?}{=}$ Bits AUDible ← BAUD named after Émile Baudot

BAUD rate = SYMBOL rate

Bit rate = BAUD rate x # of bits per symbol

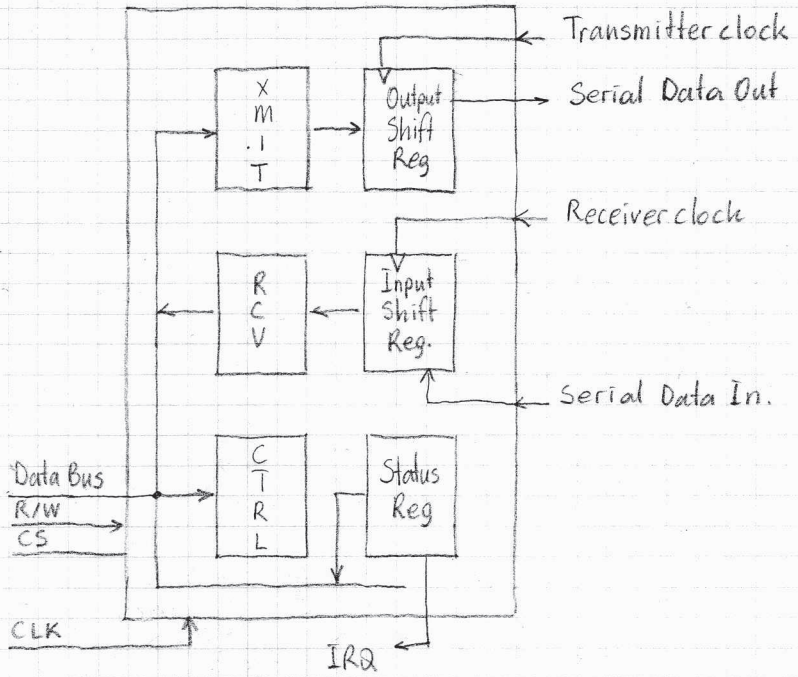
Ex Satellite TV 12.5 Msps with QPSK (2 bits/symbol)

→ bit rate 25 mbps

SERIAL INTERFACING

* Interfacing μcomputers to devices.
* Simplest electrical interface to implement
* Need PARALLEL → SERIAL conversion followed by SERIAL-PARALLEL conversion.

Typical structure of a serial port:



* RCV buffer MUST: Contents of the input shift register need to be stored immediately after the completion of a shift. Next byte might otherwise destroy recently received datum.
* XMIT buffer: Not compulsory, but improves performance.

5.1. SERIAL I/O PROTOCOLS

1. Asynchronous Protocols: Consecutive datum appear at arbitrary times.
2. Synchronous Protocols: Datum in a sequence appear at times defined by a master clock.

- 8 bit characters, usually.
- Asynchronous protocol → ASYNC between characters SYNC within character.
  * Simple, no state information required
  * Slow, 20% overhead for control information
- Synchronous protocol:
  * Fast: Combine group of characters for transmission
  * Complex: More involved receiver & transmitter.

- Asynchronous Protocols: Very poor error detection & correction
  * Parity might be used. Provides no correction info. Fails when an even # of bits are erroneous.
  * Error correction might be included in a set of characters, but is not a property of the basic protocol.
  * Character re-transmission not possible.
- Synchronous protocols
  * Redundancy might be included in blocks for error correction.
  * Blocks might include identification numbers, which enable block retransmission.
  * Provide efficient utilization of communication bandwidth.

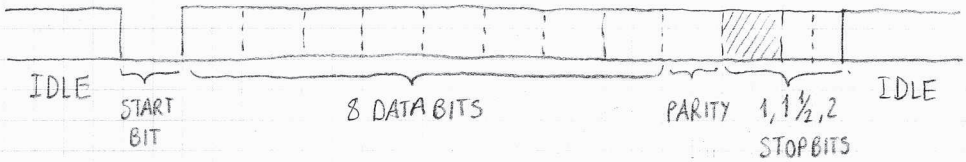
5.2 ASYNCHRONOUS PROTOCOLS

1. RS-232-C
2. 20 mA current loop.
3. RS-422, RS-423 and RS-449.

RS: Recomended Standard

EIA: Electronic Industries Association.

Bit timing for single data byte:

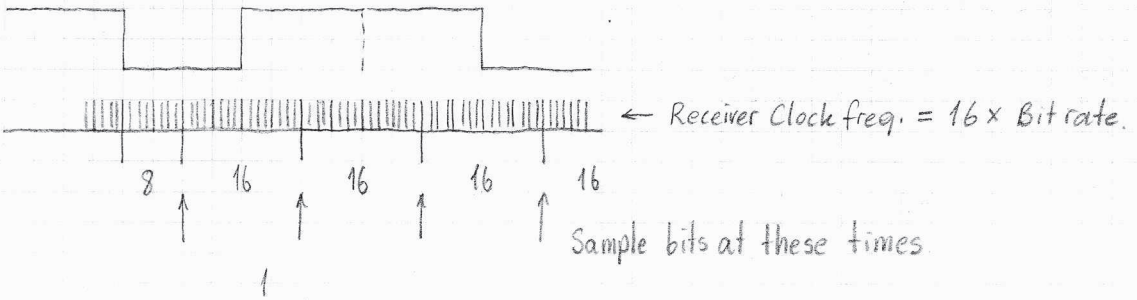


Reception Strategy:

* Determine transition for the start bit.
* Sample bits close to their mid points.
* Clock accuracy: Less than half period error for 10 bits → 5%

  12 bits 12·Error < ½ Error < 4%

Determining centers of bits



1

* 1 Start bit 1½ stop ⇒ 20% overhead 10 bits for 8
* Even worse if idle periods required for re-synchronization

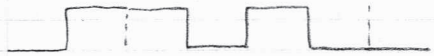
The RS-232-C Interface

Originally developed for communications over the telephone network.

MODULATION - DEMODULATION required.

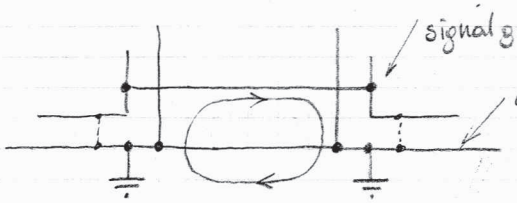
300 baud PSK
caller 1070/1270
answering 2025/2225

1 bit per symbol

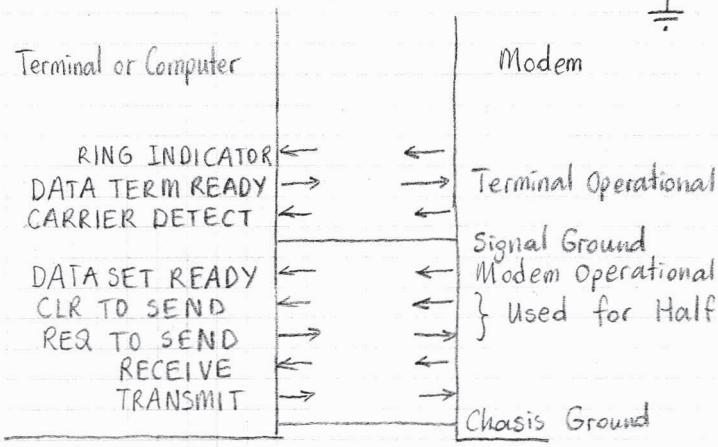


FSK → Frequency Shift Keying.

Critical Problem: GROUND LOOPS.



d < 100 feet (30 m.)

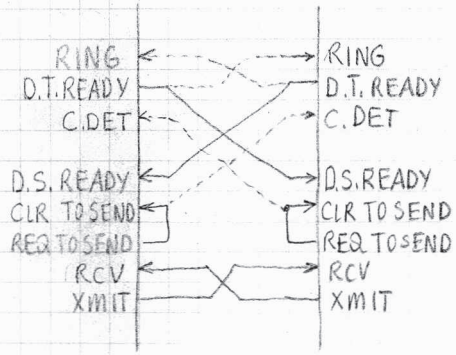


RING ← from telephone line ← Asserted during ring. Terminal should become ready for connection.

CARRIER DETECT ← Connection Active

} Telephone functions

Problem: Connecting two terminals directly:



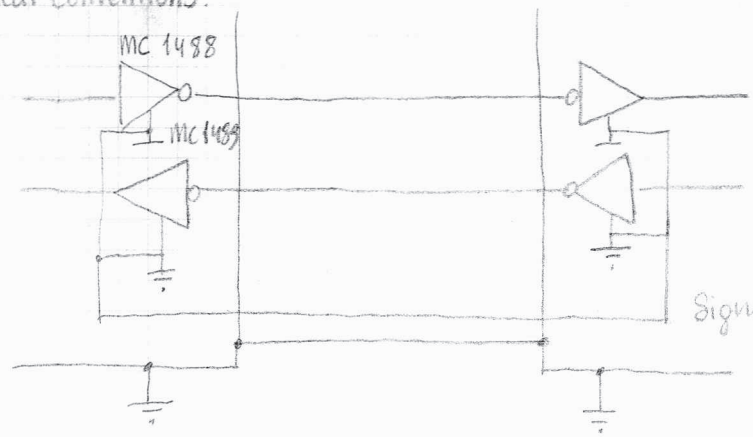
MAX 232

MC 1488 Output ±12, ±15V for noise immunity

TTL 0.8 LOW, 2.0 HIGH } 1.2 V

Margin not safe for high noise

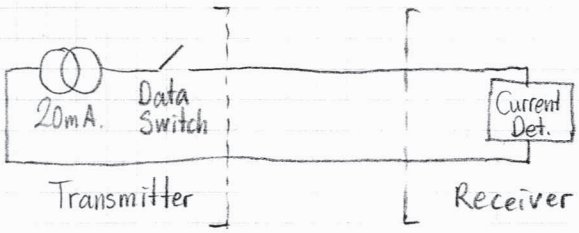
Electrical Conventions:



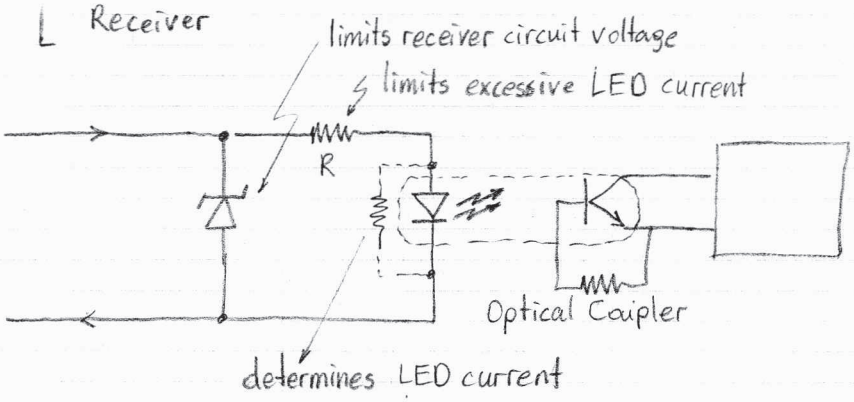
RS-232-C 20 kHz d < 30m.

20 mA CURRENT LOOP

* Originally developed for teletypes → Passive printing devices



Typical receiver circuit



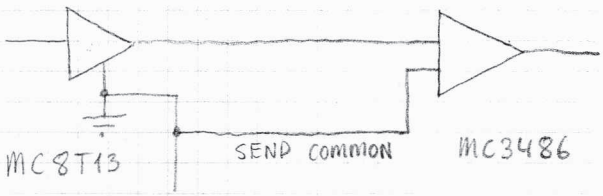
* Advantages
  - Common mode noise rejected
  - Electrical isolation (2-3 kV) → longer cables.
* Interfaces usually contain current output also.

* Disadvantage
  - No standard maintained

RS-422, RS-423 and RS-449 Interfaces

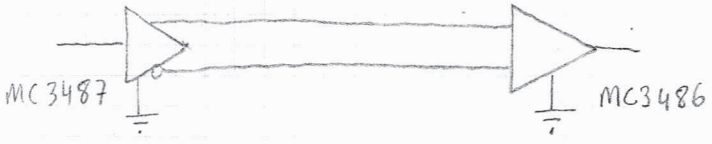
RS-422 Balanced > 20 kHz

RS-423 Unbalanced < 20 kHz → Compatible with existing standarts. RS-232-C



1 -0.2 to -6.0 V
0 0.2 to 6.0 V

RS-423

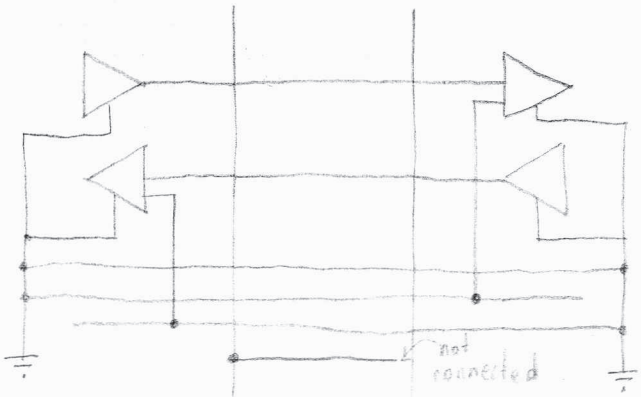


RS-422

RS-449 → 37 pin connector standart

provides for a 9-pin connector for additional channels

When RS-423 is connected to RS-232-C → Tie SEND COMMON to SIGNAL GROUND.



Unbalanced RS-423
RS-449 Standard

Signal Ground isolated from shield ground.
lenght ~60m

RS-449 SIGNALS

RECEIVE READY → Data terminal ready
DATA MODE → Data Set Ready
TEST MODE → Loopback connections - test mode
REQ TO SEND
CLR TO SEND
RCV DATA
SEND DATA
SEND COMMON
RCV COMMON
SIGNAL GROUND

Additional 9-pin connector for next channel

RCVER READY
REQ/CLR to SEND
REC/XMIT
4 ground, shield

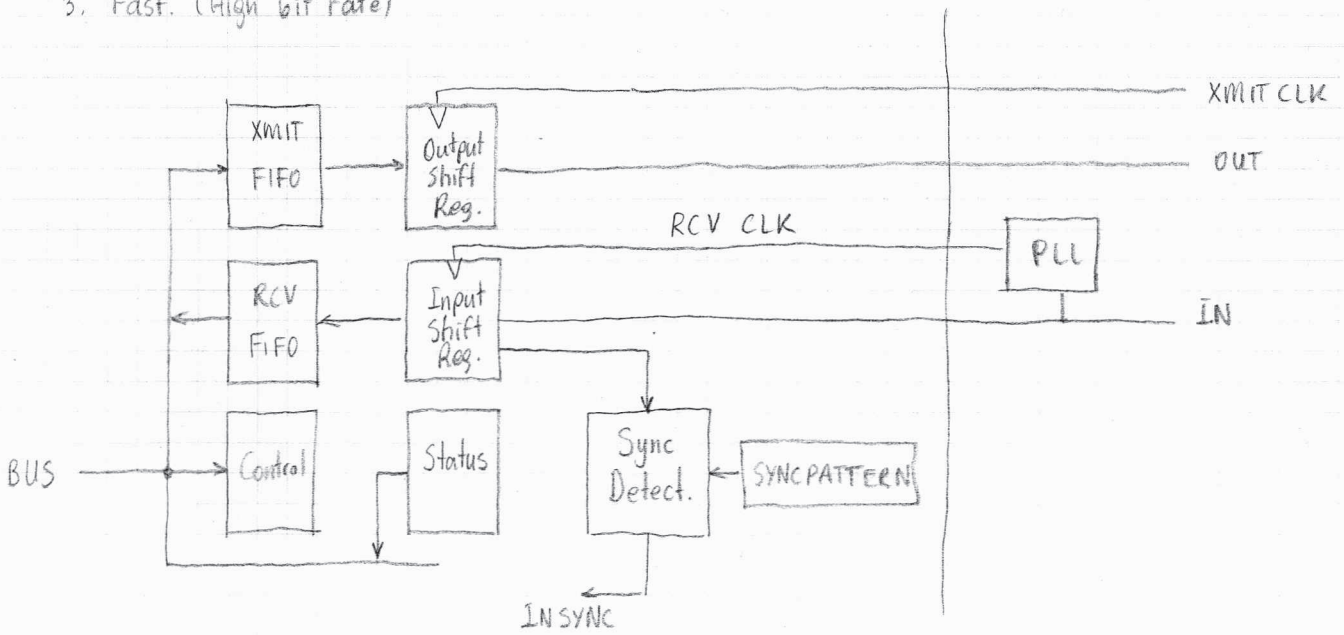
Single Ended does not comply with RS-422

Other signals: Clock, telephone network, testing

5.3 SYNCHRONOUS INTERFACES

Advantages

1. No start/stop bits → Higher bandwidth for data.
2. Block oriented → Control and error correction redundancy.
3. Fast. (High bit rate)



* Block should start with synchronization info → Also provides character synchronization.
* Includes FIFO. More bytes during single µP→port transaction. FIFO able to notify that its empty